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10EE764

Seventh Semester B.E. Degree Examination, Jan./Feb. 2021

VLSI Circuits and Design

Time: 3 hrs. Max. Marks:100

Note:* 1. *Answer any FIVE full questions, selecting at least TWO questions from each part.
2. *Missing data suitably assumed.*

PART – A

1 a. Explain Moore's law with graph. **(04 Marks)**

b. Explain in detail the n-well process of fabrication. Draw the cross sectional view of n-well CMOS inverter. **(10 Marks)**

c. Write a note on production of E-beam masks. **(06 Marks)**

2 a. Explain drain-to-source current voltage relationships for non-saturated and saturated regions. **(10 Marks)**

b. Explain the transfer characteristic in β ratio for a CMOS inverter. **(10 Marks)**

3 a. With relevant diagrams, explain the Lambda based design rules as applicable to p-well CMOS process. **(10 Marks)**

b. Explain in brief the MOS layers. Draw the stick diagram and layout for an NMOS two way selector, with enable input. **(10 Marks)**

4 a. Discuss the time constants in VLSI circuits, with an example of inverter delay. **(10 Marks)**

b. What is area capacitance and standard unit of capacitance? Calculate the total area capacitance for the multilayered structure shown in Fig.Q4(b). Assume for 5 μm technology. Also calculate the C_{in} and C_{out} values of the capacitances for the given structure:

(i) Metal 1 to substrate: 0.075×10^{-4} pF/μm^2

(ii) Polysilicon to substrate : 0.1×10^{-4} pF/μm^2

(iii) Gate to channel : 1×10^{-4} pF/μm^2

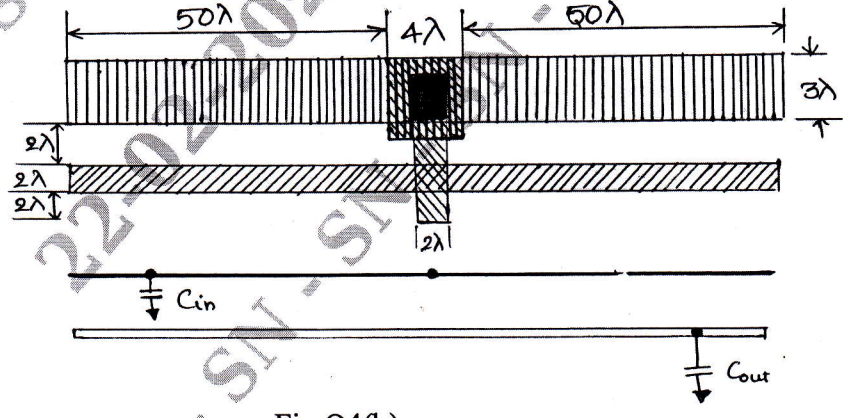

Fig.Q4(b) **(10 Marks)**

PART – B

5 a. What are different scaling models? Indicate the scaling factors for the device parameters. **(10 Marks)**

b. Discuss limitation of scaling for logic levels and supply voltage due to noise. **(10 Marks)**

6 a. Explain in detail: (i) Pseudo nMOS logic (ii) Dynamic cMOS logic (10 Marks)
b. Explain the structured design of bus arbitration logic for n lines. Also, write the circuit diagram and the stick diagram for a single cell. (10 Marks)

7 a. Explain the general arrangement of a 4-bit arithmetic processor. (10 Marks)
b. Explain the operation of 4 × 4 cross bar switch with a neat diagram. (10 Marks)

8 a. Define regularity. Explain some observations on the design process. (10 Marks)
b. With a neat diagram and relevant expressions, explain the implementation of a 4 bit ALU, using full adders. (10 Marks)

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